WHAT IS CLAIMED IS:

1. A hybrid field effect transistor package for use in a power circuit, comprising:

a gate contact;

a source contact;

a drain contact;

a silicon carbide semiconductor die consists of one of a junction field effect transistor and a metal semiconductor field effect transistor, the silicon carbide semiconductor die having three electrodes including a source electrode, a gate electrode and a drain electrode, each of the three electrodes being on one of a top surface and a bottom surface of the silicon carbide die and the drain electrode being electrically connected to the drain contact; and

a silicon metal oxide semiconductor field effect transistor comprising a doped silicon substrate and three electrodes including a source electrode, a gate electrode and a drain electrode, each of the three electrodes being on one of an upper surface and a lower surface of the silicon transistor, the gate electrode of the silicon transistor being electrically connected to the gate contact, the drain electrode of the silicon transistor being electrically connected with the source electrode of the silicon carbide die and the source electrode of the silicon transistor being electrically connected to both the source contact and the gate electrode of the silicon carbide die;

wherein one of the three electrodes of the silicon carbide die is mounted over at least a portion of one of the three electrodes of the silicon transistor or one of the three electrodes of the silicon transistor is mounted over at least a portion of one of the three electrodes of the silicon carbide die.

2. The package of claim 1, wherein the gate electrode of the silicon carbide die is mounted on the source electrode of the silicon transistor making an electrical connection with the source electrode of the silicon transistor.

3. The package of claim 2, wherein the silicon carbide die has a periphery and the periphery of the silicon carbide die does not extend beyond an area defined by the source electrode of the silicon transistor.

4. The package of claim 1, wherein the silicon carbide die has a periphery and the drain electrode of the silicon carbide die extends beyond the periphery of the silicon carbide die, and the package further comprises an insulation layer deposited on a portion of the drain electrode of the silicon carbide die, the drain electrode of the silicon transistor being mounted on the insulation layer and over a portion of the drain electrode of the silicon carbide die.

5. The package of claim 4, wherein the drain contact is an integral portion of the drain electrode of the silicon carbide die.

6. The package of claim 4, wherein the silicon substrate has a periphery, and a portion of the drain electrode of the silicon transistor extends beyond the periphery of the silicon substrate.

7. The package of claim 6, wherein at least one wire bond electrically connects an upper surface of the portion of the drain electrode of the silicon transistor to the source electrode of the silicon carbide die.

8. The package of claim 1, wherein the source electrode of the silicon transistor is mounted on a portion of the gate electrode of the silicon carbide die and the source electrode of the silicon transistor makes an electrical connection to the gate electrode of the silicon carbide die.

9. The package of claim 8, wherein the silicon carbide die has a periphery and the drain electrode of the silicon carbide die extends beyond the periphery of the silicon carbide die.

10. The package of claim 9, wherein the drain contact is an integral portion of the drain electrode of the silicon carbide die.

11. The package of claim 1, wherein the silicon transistor has a breakdown voltage rating and the silicon carbide die has a pinch-off voltage of a source to gate junction, and the breakdown voltage rating of the silicon transistor is greater than the pinch-off voltage of the silicon carbide die.